

Analysis shows that the following rules may be used to correctly identify a transition from a given line segment of Figure 4 to an adjacent line segment to the right (calling for the output signal n of the post processor to be incremented), and a transition from a given line segment to an adjacent line segment to the left (calling for the output signal n of the post processor to be decremented):

If $\bar{D} = 0$ and $s(t) \uparrow, ++n;$

If $\bar{U} = 0$ and $r(t) \uparrow, --n,$

where the up-arrow symbol represents a rising transition.

The post processor may be realized using any of a variety of logic circuits that implement the foregoing rules. Examples of such circuits are shown in Figure 9 and Figure 10.

Referring to Figure 9, the signals \bar{U} and \bar{D} are logically ANDed together and the result is applied to the enable input of an up/down counter. The signal $s(t)$ is applied to a UCLK input of the counter, and the signal $r(t)$ is applied to a DCLK input of the counter. The output signal n of the counter is the output signal of the post processor 821. The logic gates 901 function to disable counting during normal operation.

Referring to Figure 10, the signals \bar{U} and \bar{D} are again logically ANDed together and the result is applied to the enable input of an up/down counter. In addition, the \bar{U} signal is applied to a U/D input of the counter. The signal $s(t)$ and the signal $r(t)$ are logically ORed together, and the result is applied to a CLK input of the counter. The output signal n of the counter is the output signal of the post processor. The logic gates 1001 function to disable counting during normal operation.

Assuming a postprocessing circuit like that of Figure 10, the TSAD may be simplified as shown in Figure 11. In particular, in Figure 11, the multiplier of Figure 8 is replaced by circuitry 1130, including a multiplexer and an accumulator comprising an adder and a register R . In operation, increments of $2\pi K$ are added or